2.0 GHz high-linearity second stage LNA/ driver using the ATF-52189

Application Note 5245

Introduction

Avago Technologies' ATF-52189 is a high linearity, medium power, low noise E-pHEMT FET in a low cost surface mount SOT89 package. It is suitable for high output IP3 LNA Q2 & Q3 stages or driver amplifier in receiver or transmitter designs, respectively. This short note highlights a 2.0 GHz amplifier that is suitable for adaptation into cellular infrastructure WLAN & ISM products.

The ATF-52189 is packaged in an industry standard 4-lead SOT-89. The package has two source leads with large surface areas for efficient heat dissipation and low inductance RF grounding.

This application note describes the use of the ATF-52189 in an extremely high dynamic range low noise amplifier (LNA) or buffer amplifier. The demo-board's nominal performance at 2.0 GHz are: - G = 16.9 dB and output P1dB = 27.5dBm. Without any deliberate attempt to optimize the output match for best linearity, an output intercept point (OIP_3) of 40 dBm can be easily achieved. The input and output return losses are better than 12 dB.

EPHEMT Biasing

The enhancement mode technology provides superior performance while allowing a dc grounded source amplifier with a single polarity power supply to be easily designed and built. As opposed to a typical depletion mode PHEMT where the gate must be made negative with respect to the source for proper operation, an enhancement mode PHEMT requires that the gate be made more positive than the source. Biasing an enhancement mode PHEMT is as simple as biasing a bipolar transistor. Instead of a 0.7V base to emitter voltage, the enhancement mode PHEMT requires about a 0.6V potential between the gate and source, V_{gs}, for the target drain current, Ids.

The FET family can survive greater load mismatch than equivalent HBT parts while delivering rated output power. This provides adequate ruggedness in output stages without needing the protection circuitry that is often required by HBT's. Unlike bipolar devices, GaAs PHEMT's do not exhibit the phenomenon of increased gain with temperature. This inherently protects the device against over-dissipation due to thermal runaway.

Circuit Description

Biasing is accomplished by the use of a voltage divider network consisting of R2 through R9. The voltage for the divider is derived from the drain voltage which provides a form of voltage feedback to help keep drain current constant.

L2 and C5 form the bias-decoupling network for the gate of Q1. To reduce circuit loss, especially at microwave frequencies, L2 should have the following characteristics: - high unloaded Q, (Q_{UL}) and, operated below its Self Resonant Frequency (SRF). C5, which serves as virtual ground, is dimensioned for low reactance at the operating frequency (f_{opr}). The input network consisting of C1 & L1 provide a match to Q1's gate and also impart a high pass characteristic to roll off undesirable gain increase below the operating frequency. The combination of R1 and C7 in the gate bias circuit enhances Q1's stability by terminating the gate resistively at low frequency.

At Q1's drain, L3 and C6 form the bias-decoupling network. The values of these two components are determined using the same set of criteria as described for the input-side bias-decoupling network. The combination of C3 & L5 provides an impedance match to Q1's output and also rolls off the gain below the operating frequency. The ferrite bead chip, L4, works in conjunction with C8 to provide a resistive termination down to the tens of MHz range. Although a resistor can provide the same function, the power dissipation will be high. If the ferrite bead inductor is unavailable, L4 can be replaced with a combination of a 160 nH chip inductor and a 80 ohm chip resistor connected in parallel.

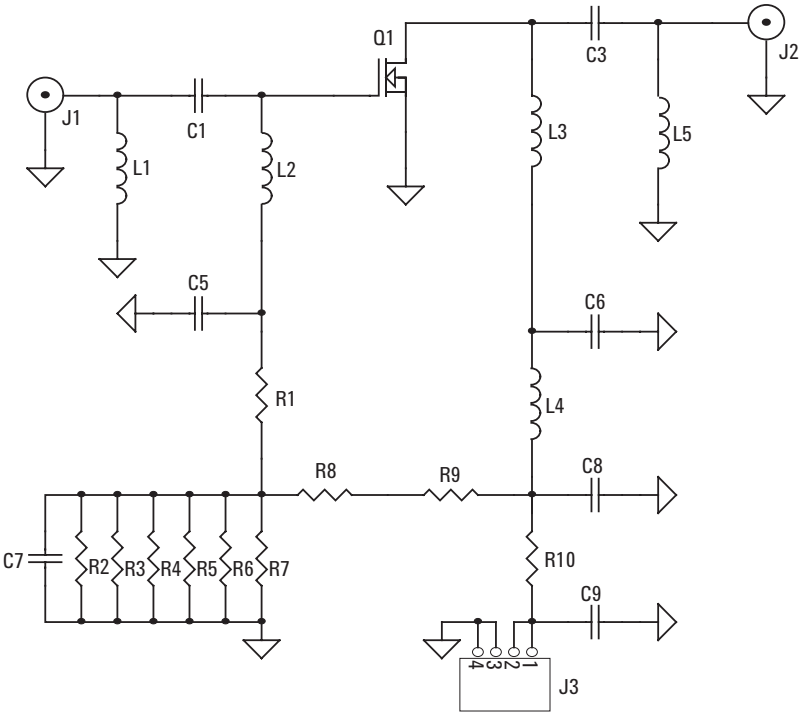

Figure 1 ATF-52189 2.4 GHz amplifier

Demoboard

A generic demonstration board is available for quick prototyping and evaluation of the ATF-52189 in the VHF through 3 GHz range. To replicate the material cost and space constraints imposed on consumer products, the demoboard was designed around low cost 0.031inch FR4 dielectric and small surface mount components. Unfortunately, the significant high frequency losses in FR4 and low Q inductors detract from the ATF-52189's true performance potential. RF connections to the demoboard are made via edge-mounted microstrip to SMA coax transitions, J1 and J2.

The demoboard requires a single 4.7 V power supply. The relatively high current (> 200 mA) drawn by the demoboard can result in appreciable voltage drop over long supply wires. The 4-pin connector, J3, permits 4-wire "Kelvin contact" to be used for compensating for voltage drop in conjunction with power supplies that support such function. If conventional 2-wire supply is used, J3's two outer leads are left unconnected.

The physical locations of inductors L1 and L5 on the demoboard have a significant effect on the return loss measurements at the input and output, respectively. If necessary, L1 and L5 can be slid a short distance along the microstrip traces to fine-tune either the input or output match, respectively. The nominal positions of these two inductors are depicted in the component placement legend.

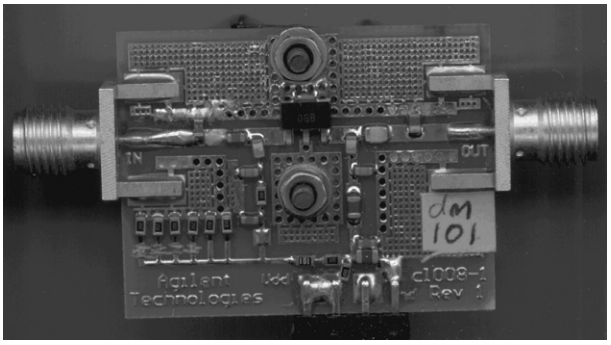

Figure 2. Fully assembled demoboard with PCB-edge mounted SMA connectors

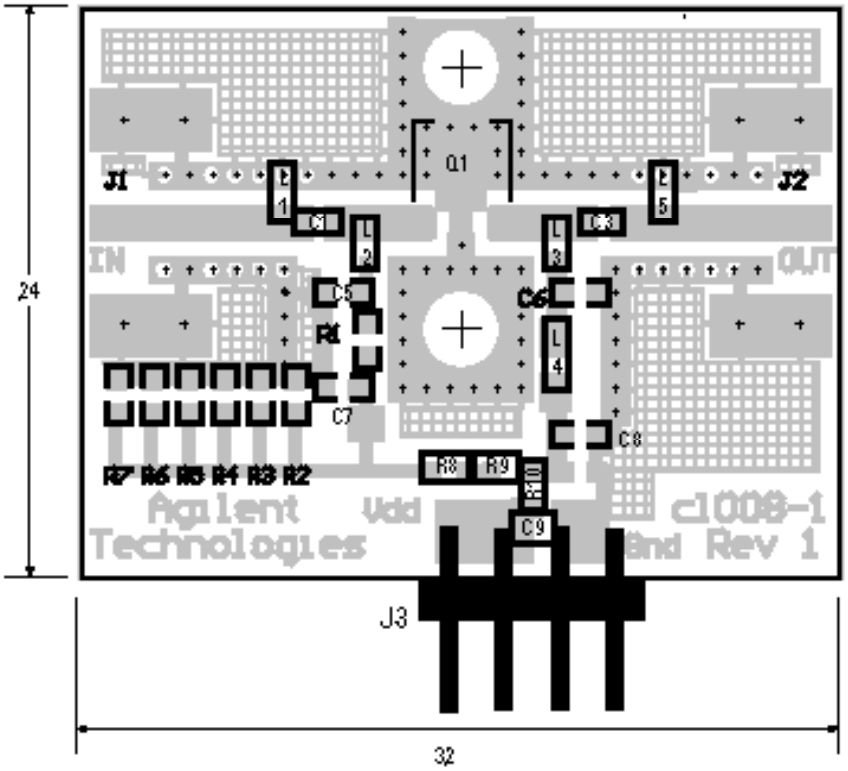

Figure 3. Component layout legend

Just like bipolar transistors, which exhibit a wide variation in HFE within a particular part number, the ATF-52189's forward transconductance, g_m, can vary from unit to unit. The resistor network, R3~R7, on the demoboard allows fine-tuning the gate bias, Vg, to cover the range of g_m variation. The individual PCB traces connecting to R3~R7 are cut one at a time until the demoboard draws the target current range of 222 ± 15 mA. This results in V_{ds} = 4.5 volt and I_{ds} = 200mA at the device-under-test, Q1.

A small segment of the PCB trace leading to the positive supply needs to be cut to fit in the resistor, R10. The position of the cut is illustrated in the demoboard's drawing. The current drawn by the demoboard can be conveniently determined from the voltage drop measured across R10. The combination of C9, R10 and C8 also limit turn-on spikes if long wires are used to connect to the power supply.

Two 3mm holes are provided for mounting a heat sink to the ground plane on the opposite side of the demoboard. Multiple via-holes around Q1, conduct heat to the ground plane and heat sink interface. To reduce the interface's thermal resistance, apply a thin layer of silicon grease thermal compound and tighten mounting screws with the correct torque recommended by the heat sink manufacturer (usually slightly beyond finger tight).

Circuit Simulation

An RF simulator like Avago Technologies' ADS allows the input and output tuning networks to be dimensioned with fewer "cut & try" iterations. In addition, critical parameters such as stability and gain can be predicted during the preliminary design stage. For example, if the simulation forecasts a strong tendency to self-oscillation, the designer can pre-empt the problem by incorporating additional stabilization components into the preliminary circuit.

There is no need for customers to carry out their own preliminary characterization of the ATF-52189 as the Touchstone formatted "s2p" files at various DC biasing can be downloaded from the Avago Technologies website. www.avagotech.com

Real-world components are inescapably blighted by parasitics that cause a frequency-dependent variation of the electrical characteristics. Above VHF, the correlation between the simulated results and measured data hinges on how detailed the equivalent circuit is; in other words, how completely the component models account for the parasitic effects. Some passive component manufacturers can supply either s-parameter data or model libraries for their products. For example, Murata provides an ADS model library for chip capacitors and this removes the modeling burden from the circuit designer. However, there is generally an upper frequency limit to most manufacturers SPAR and when ADS extracts them above this frequency, simulated circuit performance will not be correct.

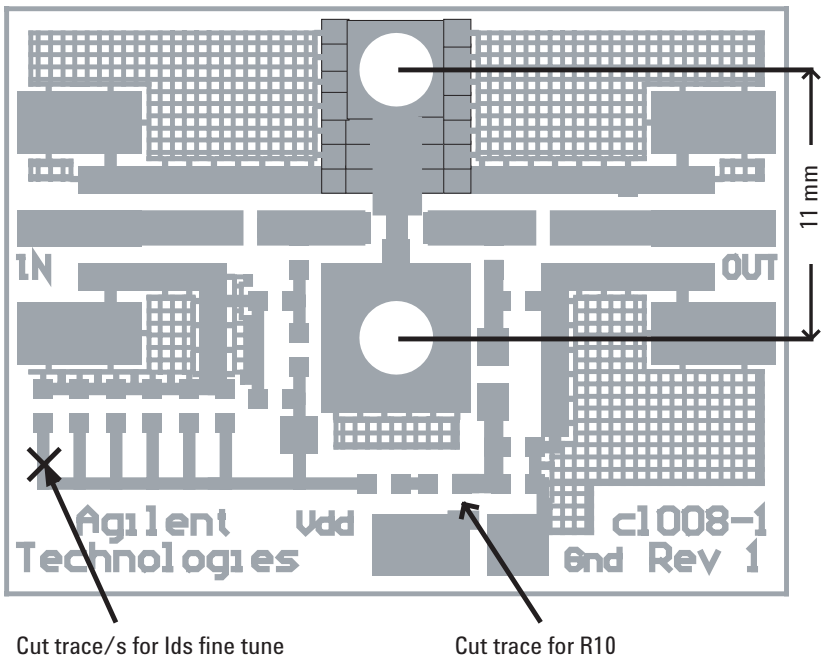

Figure 4. Positions of PCB trace cuts and distance between heatsink screws

For other components like inductors and resistors, the designer may have to create the model himself. Unfortunately, if every parasitic element were to be accounted for exhaustively, the equivalent circuit will become unwieldy complicated. To strike a balance between simulation time and accuracy, only the components' and PCB's most significant first-order parasitic are included in their respective models. For example, when a ground return path consists of many via-holes in parallel, the resultant parasitic approximates ideal ground. So, the via-holes can be excluded from the simulated circuit without adversely affecting the accuracy. Similar generalization can be made for other components. Low value resistors (< 50 ohm) can be approximated by a resistor and a parasitic inductor connected in series. The parasitic parallel capacitive reactance can be conveniently ignored, as the small resistance is affected by the series inductive reactance to a greater degree. In contrast, a high value resistor (> 50 ohm) is more sensitive to the parallel capacitive parasitic than the series inductive parasitic. A good tutorial on simplifying the models of lumped components can be found in Randall Rhea's "Oscillator Design and Computer Simulation" (Chap. 1, "Analysis Fundamentals").

During actual tuning on the demoboard, the trajectories of the input-matching network can be empirically verified against simulation in a 'component-by-component' manner. The manual tuning process is more intuitive if the matching components can be made to move along predictable paths on the Smith Chart (e.g. reactances move along constant resistance or constant admittance circles). To make this happen, the phase shift between the end of the test cable to the matching network has to be mathematically compensated out using either one of the Network Analyzer's built-in functions: linear phase compensation, normalization or time domain gating.

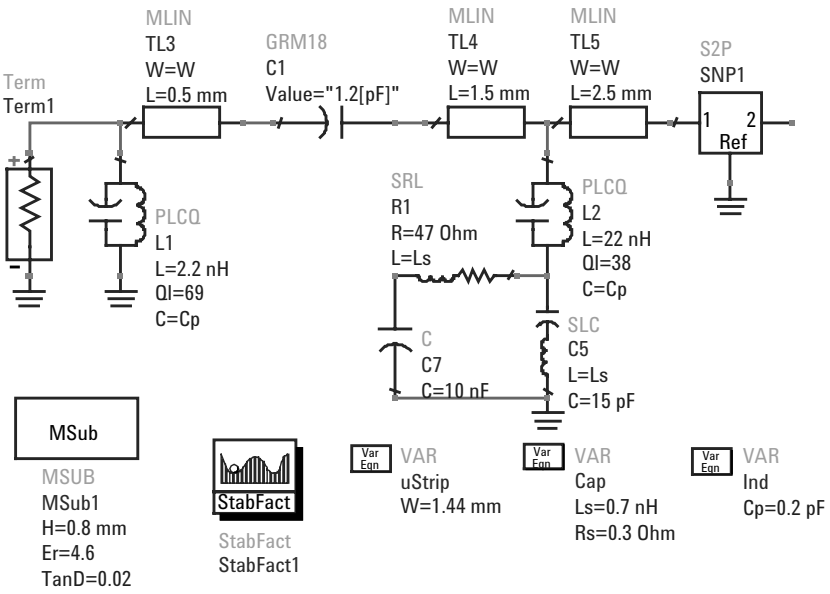

Figure 5. Input matching & biasing networks

The measured trajectories of the input match are shown below. The curve annotated with the marker "1" represents the impedance of the ATF-53189's input after being phase-shifted by a short length of microstrip (represented by TL5 in the simulation) to the approximate position of the matching network. The addition of C1 moves the input-side impedance along the constant resistance circle to "2". The shunt inductor, L1, shifts point "2" to the final position "3" near to the Smith chart centre whilst traveling along the constant admittance circle.

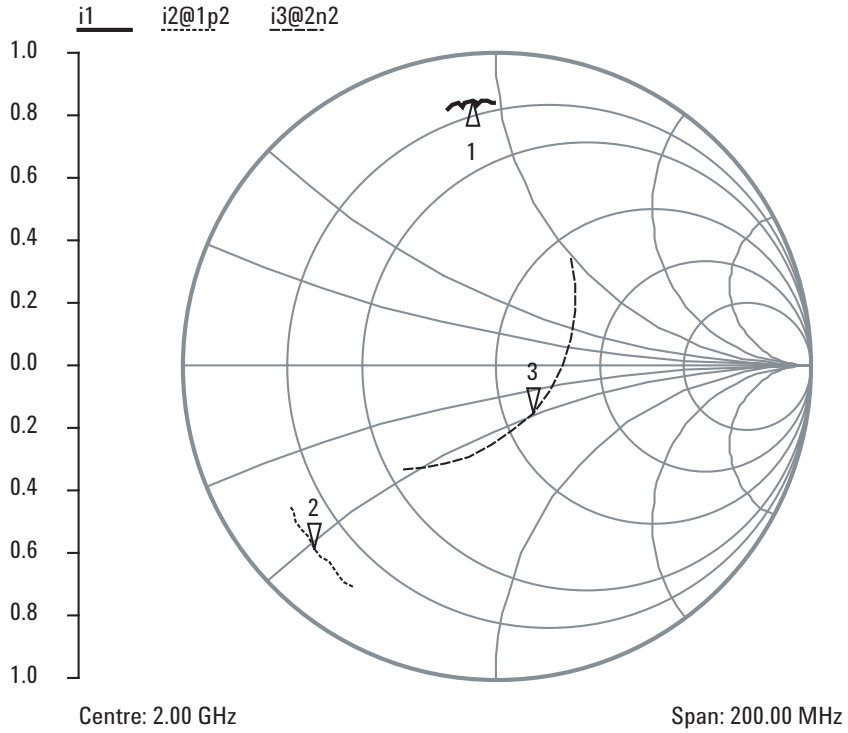

Figure 6. Measured trajectories of input impedance during the various phases of matching

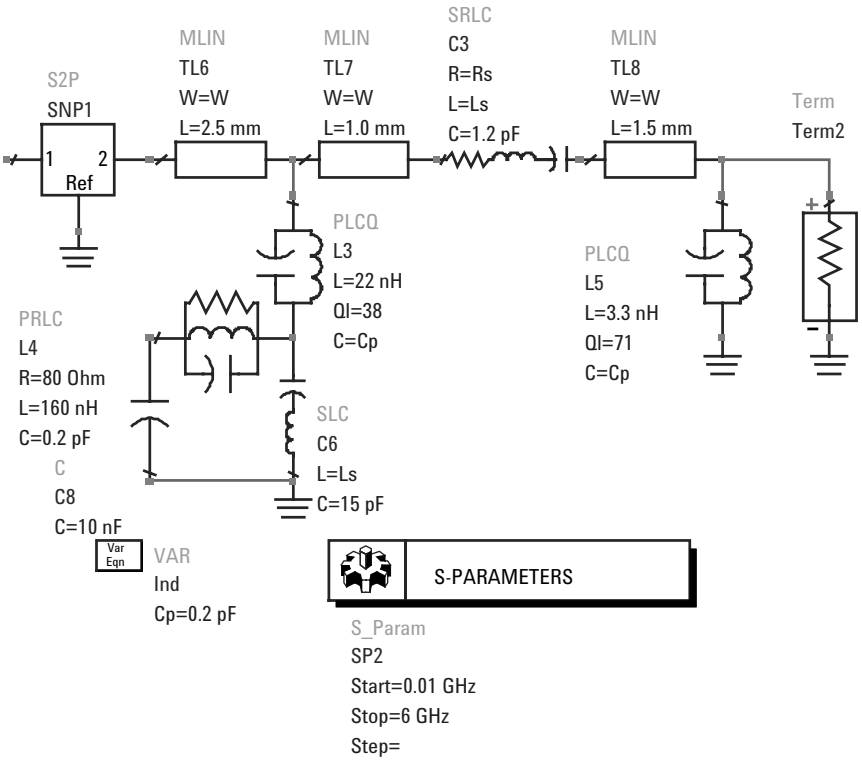

Figure 7. Output biasing and matching circuit

The measured trajectories of the output match are shown below. The curve annotated with marker "1" represents the ATF-52189's drain impedance after being phase-shifted to the approximate position of the output matching network by the connecting microstrip trace (TL6 in simulation). Subsequently, the addition of C3 moves the trace along the constant resistance circle to "2". The last matching component, L5 nudges the output impedance curve along the constant admittance circle to position "3" - 'wrapping around' the chart centre.

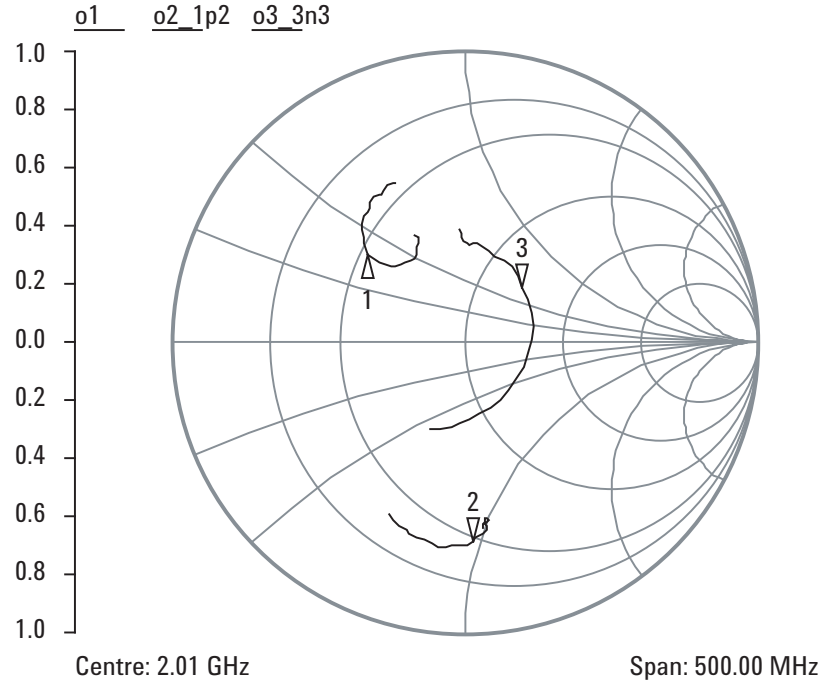

Figure 8. Measured trajectories of output impedance during the various phases of matching

Measured performance

The demoboard performance was measured under the following test conditions: - Vds = 4.5 V, Ids = 200 mA and f_c = 2.0 GHz.

The ATF-52189 is intended for either the driver amplifier, or the second-stage LNA slots, in transmit and receive chains, respectively. So, matching for minimum noise figure (NF) does not carry the same over-riding consideration as would have been in a first-stage LNA. However, good return loss over a broad bandwidth is required in these two slots. In line with this design goal, no attempt was made to tweak the input match for the lowest NF.

While satisfying the requirement for good input match, the NF can be improved, especially at higher microwave frequencies, by reducing the inevitable circuit losses. The low cost bias inductor at the input can be replaced with a higher Q component, e.g. air-cored spring wound inductor. The degradation in NF due to losses in the inductor can be estimated from: -

$$loss = 20 \log \frac{Q_u - Q_l}{Q_u}$$

Additionally, some reduction in input-side loss may be obtained by changing the PCB material from FR4 to a lower loss substrate, such as Rogers RO4350.

The ATF-52189 demoboard amplifier exhibits good input and output return losses. This minimizes detuning effects when the amplifier is cascaded with other stages in the RF chain. For example, filters and aerials are especially susceptible to the adverse effects of reflective terminations. Designing the amplifier's input and output for a close match to 50Ω over the operating bandwidth, prevents unpredictable shift in the cascaded frequency response.

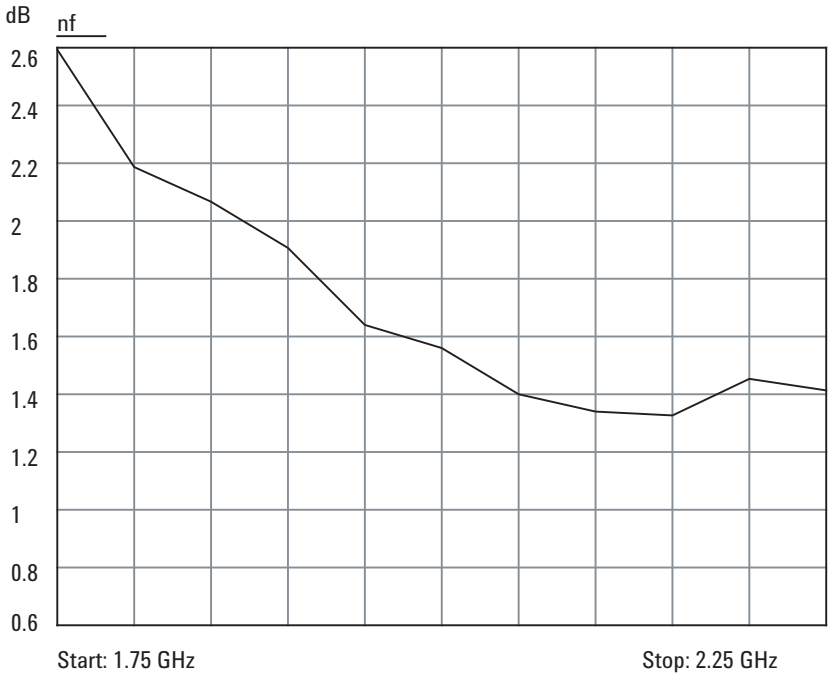

Figure 9. Measured NF

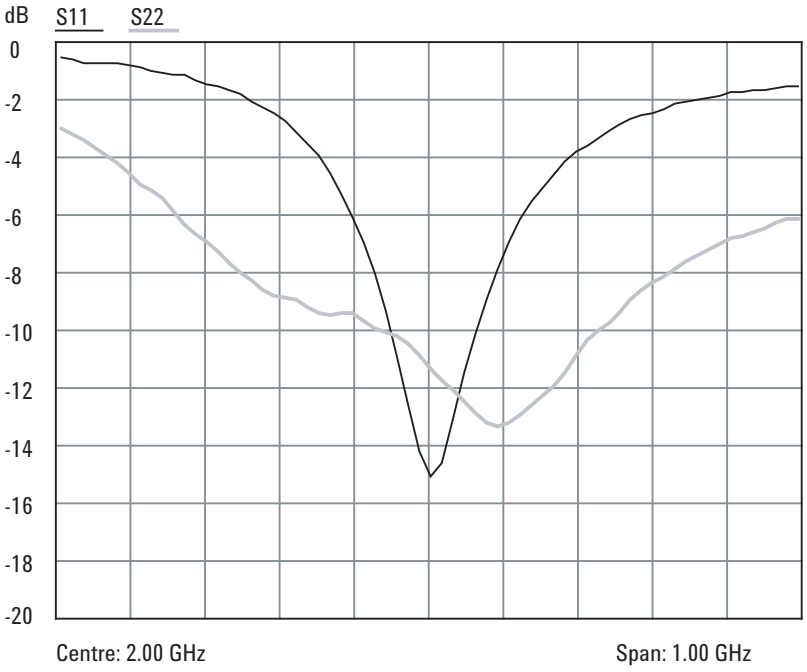

Figure 10. Measured input and output return loss

The gain was approximately 16.9 dB in the middle of the pass-band. Slightly more gain can be obtained at the expense of higher cost by using high Q inductors and/or a PCB substrate with lower loss.

The 1 dB gain compression point, P_{1dB}, indicates the upper limit of either the input or the output power level at which saturation has started to occur. As the output power approaches this limit, non-linearities in the amplitude transfer function cause a rapid growth of inter-modulation products. Linear modulation schemes, both analogue and digital, require some amount of backing off from saturated operation. Unfortunately, efficiency drops rapidly when the amplifier is operated further below the clipping threshold.

In digital communication, back-off may be implemented to reduce spectral regrowth. Different wireless standards mandate spectral masks for preventing adjacent channel interference. From published literatures, the suggested amount of back-off from the cw P1dB in order to comply with Adjacent Channel Power (ACP) specification ranges from 0 dB in IS-137 TDMA[1] to > 3 dB in GSM EDGE[2].

The P_{1dB} is measured by progressively increasing the input power while noting the point when the gain became compressed by 1 dB. P_{1dB} is customarily referred to the output. In the ATF-52189 demoboard, the 1dB & 3dB gain compression typically occur at 27.4 dBm and 28.3 dBm, respectively.

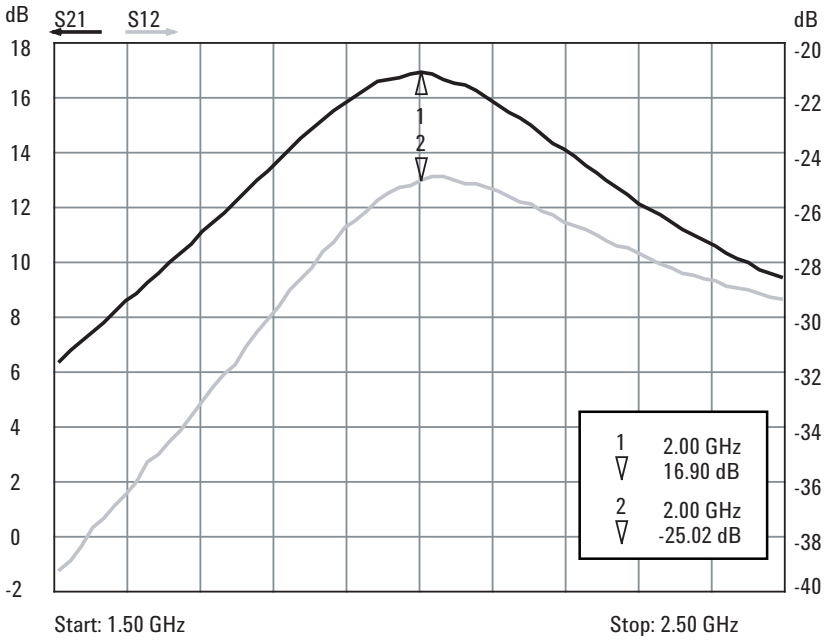

Figure 11. Measured forward gain and reverse isolation

1 B. Aleiner, "Correlation between PldB and ACP in TDMA Power Amplifiers", Applied Microwave & RF, Mar. 1999.
2 S.C. Cripps, "RF Power 2005", Microwave Journal, Apr. 2005.

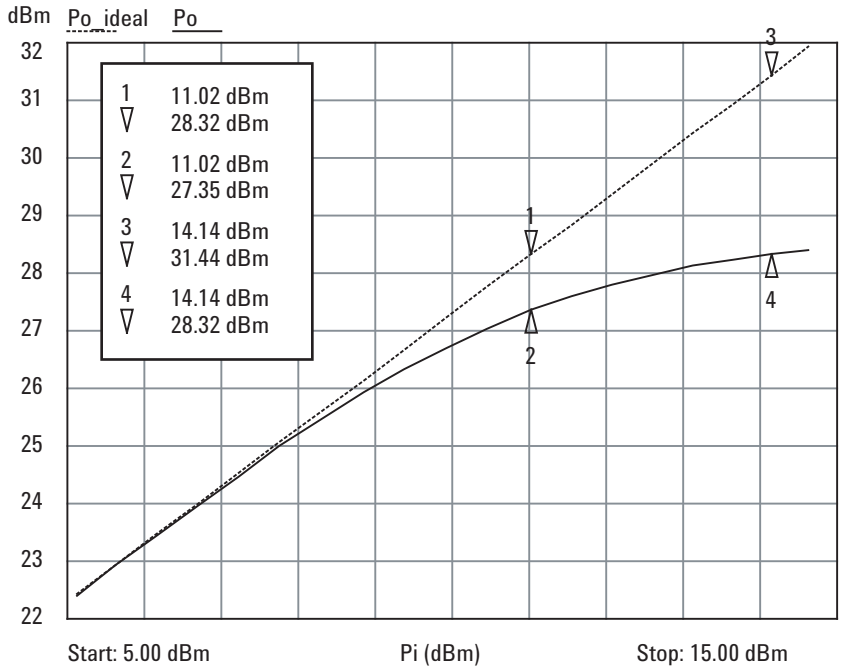

Figure 12. Theoretical & Measured Output Power Vs. Input Power

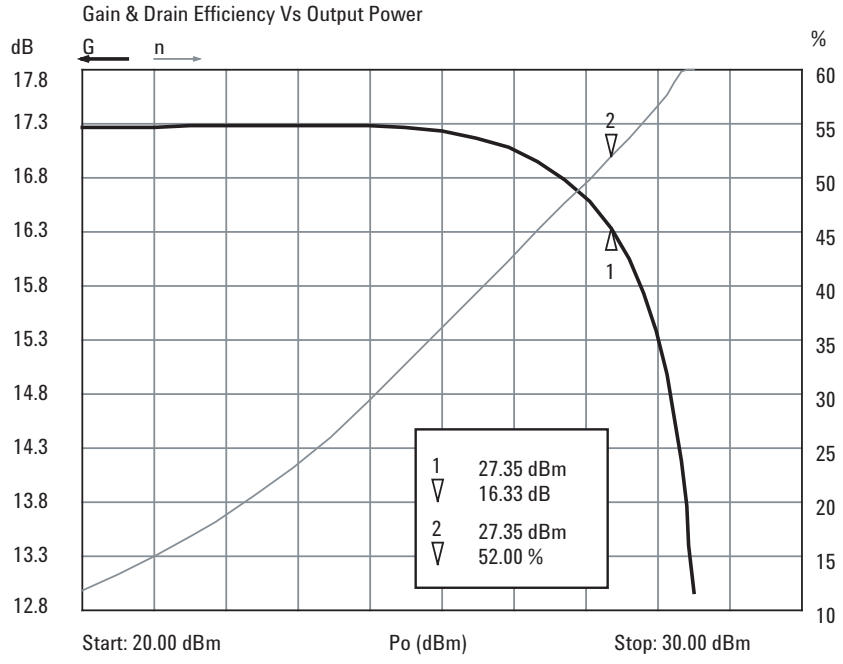

Figure 13. Measured gain vs. output power

The gain and the drain efficiency are plotted against the output power on the same graph. This allows the designer to juggle between efficiency and the amount of back-off dictated by the modulation scheme's Peak to Average power Ratio (PAR). The drain efficiency at the 1 dB compression point, h_{1dB}, is approximately 52%.

The intercept point is another measure of amplifier linearity. The theoretical point when the fundamental signal and the third order intermodulation distortion are of equal amplitude is the third order intercept point, IP_3. The distortion level at other power levels can be conveniently calculated from the amplifier's IP_3 specification.

Two test signals spaced 5 MHz apart were used for evaluating the ATF-52189 demoboard. The large dynamic range between the fundamental tones and the intermodulation products meant that the latter is barely above the spectrum analyzer's noise floor. To measure the 3rd order product amplitude accurately, a very narrow sweep span can be used to improve the signal to noise ratio. As a tradeoff from the narrow sweep span, only one fundamental and one 3rd order intermodulation output signals can be practically displayed on the graph. Both the fundamental and intermodulation tones are overlaid over the same frequency axis for amplitude comparison purpose. The IP_3, referenced to the output, can be calculated from: -

$$IP_3 = P_{fund} + \frac{\Delta IM}{2}$$

where P_{fund} is the amplitude of either one of the fundamental outputs, and ΔM is the amplitude difference between the fundamental tones and the intermodulation products.

The output intercept point, OIP_3, is approximately 40dBm.

Like all microwave transistors, the ATF-52189 demonstrates increasing gain corresponding with decreasing frequency. If this phenomenon is not tamed with the appropriate countermeasures, the amplifier can break into self-oscillation below its operating frequency - in the tens of MHz range. To assess the effectiveness of the low frequency circuit stabilization described previously, the Rollett stability criterion was calculated from the measurement of the demoboard's s-parameters. The ATF-52189 demoboard exhibits unconditional stability (k >1) over the range of frequencies that an 8753 network analyzer is capable of operating. This reduces the design effort required to adapt the ATF-52189 into the final product.

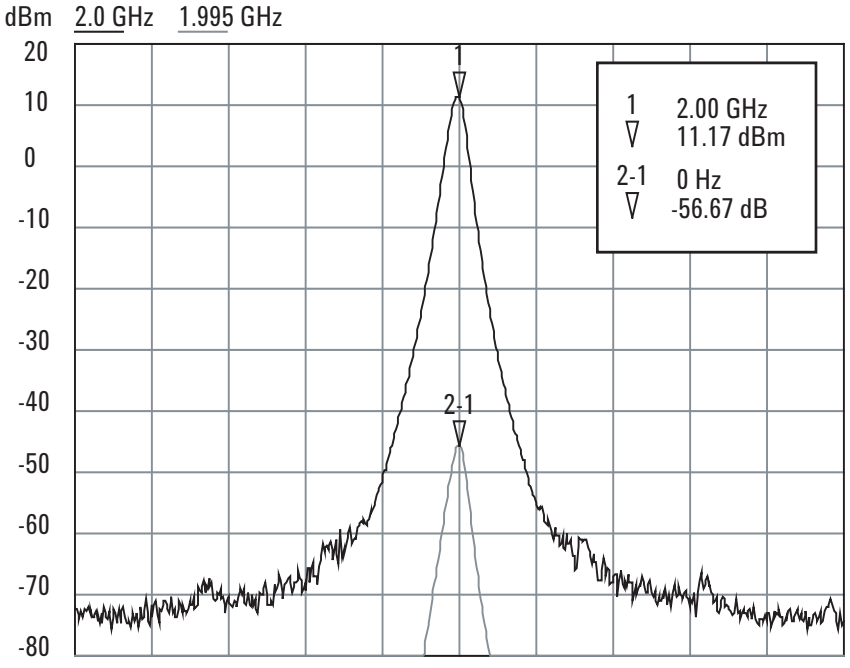

Figure 14. Fundamental tone and lower intermodulation product overlaid over the same freq. axis

Inadvertent coupling between the amplifier's input and output and component parasitic can lead to instability in the upper microwave region. If there are pronounced gain peaks above its operating frequency, the amplifier may oscillate under certain operating conditions. In a wideband sweep test of the ATF-52189 demoboard up to 20 GHz, no abnormal peak was recorded in the frequency response.

The nominal performance of the ATF-52189 demoboard is summarized below: -

Table 1. Demoboard nominal performance values

Vsupply (V)	4.7
Isupply (mA)	225
Fc (MHz)	2000
G (dB)	16.9
RL in (dB)	< -10
RL in (dB)	< -10
k	> 1
P1dB (dBm)	27.5
OIP3 (dBm)	40

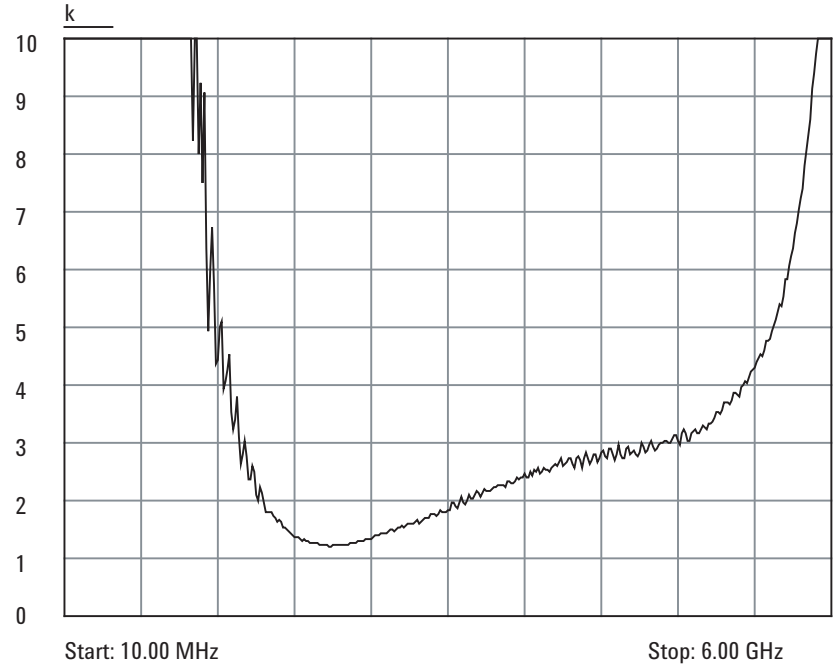

Figure 15. Stability (k) calculated from measured s-parameters

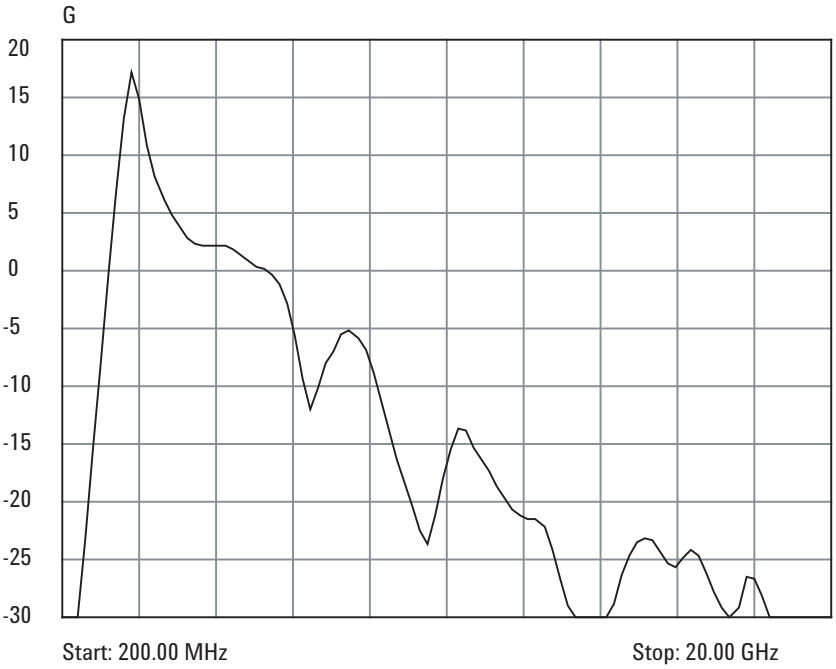

Figure 16. Wideband gain sweep

Demoboard part list

The demoboard's table of components is listed below. L3 is a ferrite bead inductor in surface mount package.

Table 2: List of components

Pos.	Value	Size	Description	Manufacturer
C1	1.2 pF	0603		Murata
C3	1.2 pF	0603		Murata
C5	15 pF	0603		Murata
C6	15 pF	0603		Murata
C7	10 nF	0603		Murata
C8	10 nF	0603		Murata
C9	2.2 uF	0603		Murata
J1	SMA conn.		0.8mm Pcb edge mount	
J2	SMA conn.		0.8mm Pcb edge mount	
J3	4 pin header		2.54mm spacing	
L1	2.2 nH	0603	LL1608	Toko
L2	22 nH	0603	LL1608	Toko
L3	22 nH	0603	LL1608	Toko
L4	60 R	0805	BLM21PG600SN1D Ferr. Bd.	Murata
L5	3.3 nH	0603	LL1608	Toko
Q1	ATF-52189			Agilent
R1	47 R	0603		
R2	27 R	0603		
R3	560R	0603		
R4	560R	0603		
R5	560R	0603		
R6	560R	0603		
R7	560R	0603		
R8	180 R	0603		
R9	0 R	0603		
R10	1 R	0603		

Active bias

Passive biasing was used in this application note solely for prototyping convenience. Every demoboard will need individual adjustment of its resistor divider. For this reason, passive bias should not be considered for anything more than a one-off prototype. Active biasing is imperative for the ATF-52189 amplifier in volume production. Active biasing offers the ability to hold the drain to source current constant over variations in both g_m and temperature. A very inexpensive method of accomplishing this is to use two PNP bipolar transistors arranged in a pseudo-current mirror configuration.

Transistor Q1 is configured with its base and collector tied together. This acts as a simple PN junction, which helps temperature compensate the Emitter-Base junction of Q2.

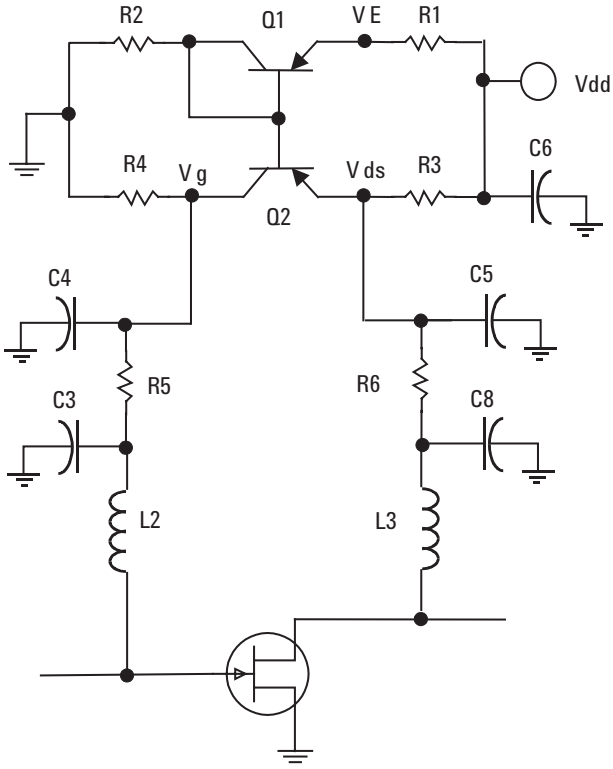

Figure 17. Typical active bias applied to a FET transistor

To calculate the values of R1, R2, R3, and R4 the following parameters must be known or chosen first:

I_{ds} is the device drain-to-source current;

I_R is the Reference current for active bias;

V_{dd} is the power supply voltage available;

V_{ds} is the device drain-to-source voltage;

V_g is the typical gate bias;

V_{be1} is the typical Base-Emitter turn on voltage for Q1 & Q2;

Therefore, resistor R3, which sets the desired device drain current, is calculated as follows:

$$R3 = \frac{V_{dd} - V_{ds}}{I_{ds} + I_{c2}}$$

where, I_{C2} is chosen for stability to be 10 times the typical gate current and also equal to the reference current I_R (which flows through R2). R4 acts as a load to keep current flowing through Q2.

The next three equations are used to calculate the rest of the biasing resistors.

Note that the voltage drop across R1 must be set equal to the voltage drop across R3, but with a current of I_R.

$$R1 = \frac{V_{dd} - V_{ds}}{IR} \quad (5)$$

R2 sets the bias current through Q1.

$$R2 = \frac{V_{ds} - V_{be1}}{IR} \quad (6)$$

The FET drain current forces a Vg which is placed across R4 which then determines I_{C2}.

$$R4 = \frac{Vg}{IC_2} \quad (7)$$

The drain current is regulated by R3 being placed between a regulated supply voltage of V_{dd} and the regulated voltage at the emitter of Q2 driven by the somewhat regulated voltage determined by the voltage divider R2 and R1 with a temperature compensating diode consisting of Q1 with its base and collector tied together.

For more information on active biasing, please refer to Application Note 1320 (Avago Technologies ATF-521P8 900 MHz High Linearity Amplifier). Table 1 of the aforementioned application note provides reference values for R1~ R4.

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